

REMARKS

The Official Action mailed April 3, 2008, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on April 12, 2004; September 22, 2004; and August 22, 2007.

However, the Applicant has not received acknowledgment of the Information Disclosure Statement filed on March 3, 2008 (received by OIPE March 5, 2008). The Applicant respectfully requests that the Examiner provide an initialed copy of the Form PTO-1449 evidencing consideration of the above-referenced Information Disclosure Statement.

Claims 1-42 are pending in the present application, of which claims 1, 8, 15, 22, 29 and 36 are independent. Claims 1-4, 8-11, 15-18, 22-25, 29-32 and 36-39 have been amended to better recite the features of the present invention. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 3 of the Official Action rejects claims 1-42 as obvious based on Figures 2-5 of the present application, which the Official Action refers to as "Admitted Prior Art Background of the Invention ... (hereinafter, 'APA')" and U.S. Patent No. 5,650,834 to Nakagawa. The Applicant respectfully submits that a *prima facie* case of obviousness cannot be maintained against the independent claims of the present application, as amended.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some reason, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second,

there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some reason to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims, as amended. Independent claims 1, 8, 15, 22, 29 and 36 have been amended to recite that one terminal of a thin film resistor is connected to a thin film element and the other terminal of the thin film resistor is connected to a chip capacitor. Also, independent claims 22, 29 and 36 have been amended to recite a pixel portion formed over an insulating substrate. For the reasons provided below, APA and Nakagawa, either alone or in combination, do not teach or suggest the above-referenced features of the present invention.

The Official Action concedes that "APA does not explicitly disclose: a thin film element formed over an insulating substrate; a thin film resistor formed over the insulating substrate; and a chip capacitor mounted over the insulating substrate" (page 3, Paper No. 20080117). Also, the Official Action asserts that "Nakagawa discloses ... thin film transistors ... on the transparent insulative substrate (8, Fig. 5), a plurality of gate lines (11, Fig. 5) each adapted to supply a signal to a gate electrode of each of the thin film transistors (6, Fig. 5), ... a thin film resistor provided intermediate between an input terminal of each of the signal lines and shortcircuiting ring; [and a] capacitor (3, Fig. 1; see col. 4, lines 33-53; col. 6, lines 38-60)" (Id.; emphasis added). Further, the

Official Action asserts that “[i]t would have been obvious to one of ordinary skill in the art ... to have incorporated the active-matrix substrates taught by Nakagawa with the audio signal processing circuit of APA to obtain the audio signal processing circuit claimed limitations since the claimed invention is merely a combination of old elements, and in the combination each element merely would have performed the same function as it did separately” (Id.). The Applicant respectfully disagrees and traverses the assertions in the Official Action.

Reference character 11 in Nakagawa denotes a gate insulating film (see column 9, lines 22-23) and reference character 6 in Nakagawa denotes a thin film resistor (see column 6, line 50). Therefore, the assertion in the Official Action, that the gate insulating film 11 of Nakagawa corresponds to the plurality of gate lines of the present claims, is incorrect. Also, the assertion in the Official Action, that the thin film resistor 6 of Nakagawa corresponds to the thin film transistors of the present claims, is incorrect. Rather, Nakagawa appears to teach a thin film transistor 1 over a substrate 8, a thin film resistor 6 over the substrate 8, and a capacitor 3 over the substrate 8 (see, e.g., Figures 1, 5(a) and 5(b)).

Furthermore, in order to further distinguish the present invention from the alleged combination of APA and Nakagawa and to clarify the features of the present invention, the Applicant has amended independent claims 1, 8, 15, 22, 29 and 36 to recite that one terminal of a thin film resistor is connected to a thin film element and the other terminal of the thin film resistor is connected to a chip capacitor. Unlike the conventional APA circuit using external resistors and Nakagawa, the present invention including the above features has the advantage that no parasitic low pass filters are formed by the parasitic capacitors 113 and 114 since only one of two terminals of the thin film resistor at the chip capacitor side is on the outside.

On the other hand, in Nakagawa, a thin film resistor 6 of 10k Ω to 500k Ω is provided intermediate between each of the input terminals 4a, 5a and the shortcircuiting ring 7 to serve as a shortcircuiting line for discharging static electricity in such a short

time as not to cause problems such as shifting of the threshold voltage of TFT (see column 6, line 61, to column 7, line 4). That is, Nakagawa merely discloses that one terminal of thin film resistor 6 is connected to the input terminals 4a, 5a and the other terminal of thin film resistor 6 is connected to the shortcircuiting ring 7, not the capacitor 3. The Applicant respectfully submits that it would not have been obvious to one of ordinary skill in the art at the time of the present invention to modify APA or Nakagawa so that one terminal of the thin film resistor 6 is connected to the TFT 1 through the input terminal 4a, 5a and the other terminal of thin film resistor 6 is connected to the capacitor 3 through another thin film resistor 6 and another input terminal 4a, 5a.


Further, regarding independent claims 22, 29 and 36, the Official Action asserts that "the preamble recitation of 'a display device' is given no weight since no further mention of such is made in the body of these claims" (pages 6-7, Paper No. 20080117). Thus, the Applicant has further amended independent claims 22, 29 and 36 to recite a pixel portion formed over an insulating substrate in the body of each claims. These features are supported in the present specification, for example, by Figures 8 and 9.

Therefore, the Applicant respectfully submits that APA and Nakagawa, either alone or in combination, do not teach or suggest that one terminal of a thin film resistor is connected to a thin film element and the other terminal of the thin film resistor is connected to a chip capacitor; or a pixel portion formed over an insulating substrate.

Since APA and Nakagawa do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,


Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789